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Remote Oxygen Scavenging of the Interfacial Oxide Layer in Ferroelectric Hafnium–Zirconium Oxide-Based Metal–Oxide–Semiconductor Structures

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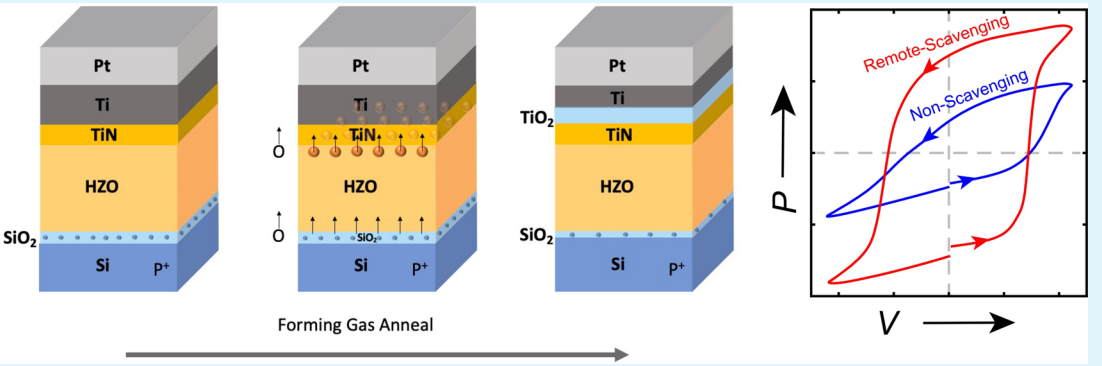

ABSTRACT: Discovery of ferroelectricity in HfO_2 has sparked a lot of interest in its use in memory and logic due to its CMOS compatibility and scalability. Devices that use ferroelectric HfO_2 are being investigated; for example, the ferroelectric field-effect transistor (FEFET) is one of the leading candidates for next generation memory technology, due to its area, energy efficiency and fast operation. In an FEFET, a ferroelectric layer is deposited on Si, with an SiO_2 layer of ∼1 nm thickness inevitably forming at the interface. This interfacial layer (IL) increases the gate voltage required to switch the polarization and write into the memory device, thereby increasing the energy required to operate FEFETs, and makes the technology incompatible with logic circuits. In this work, it is shown that a Pt/Ti/thin TiN gate electrode in a ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ based metal-oxide-semiconductor (MOS) structure can remotely scavenge oxygen from the IL, thinning it down to ∼0.5 nm. This IL reduction significantly reduces the ferroelectric polarization switching voltage with a ∼2× concomitant increase in the remnant polarization and a ∼3× increase in the abruptness of polarization switching consistent with density functional theory (DFT) calculations modeling the role of the IL layer in the gate stack electrostatics. The large increase in remnant polarization and abruptness of polarization switching are consistent with the oxygen diffusion in the scavenging process reducing oxygen vacancies in the HZO layer, thereby depinning the polarization of some of the HZO grains.

KEYWORDS: *ferroelectricity, remote-scavenging, interlayer, EOT reduction, polarization*

INTRODUCTION

Ferroelectricity in HfO_2 and its alloyed variants with the fluorite structure holds the promise to greatly impact the microelectronics of next-generation computing paradigms, including logic, memory, and neuromorphic computing.[1−6] Direct integrability of these materials on Si with reasonable interfacial quality along with their relatively moderate dielectric constants (20−30) and relatively high coercive fields (∼1 MV/cm), compared to standard perovskite oxide-based ferroelectrics, has led to the renewed interests into a device technology, called the ferroelectric field-effect transistor (FEFET), which had remained elusive for many decades.[7,8] In a FEFET, a ferroelectric layer is integrated into the gate dielectric stack in a standard transistor architecture. Due to its fast operation, nondestructive read, and energy and area

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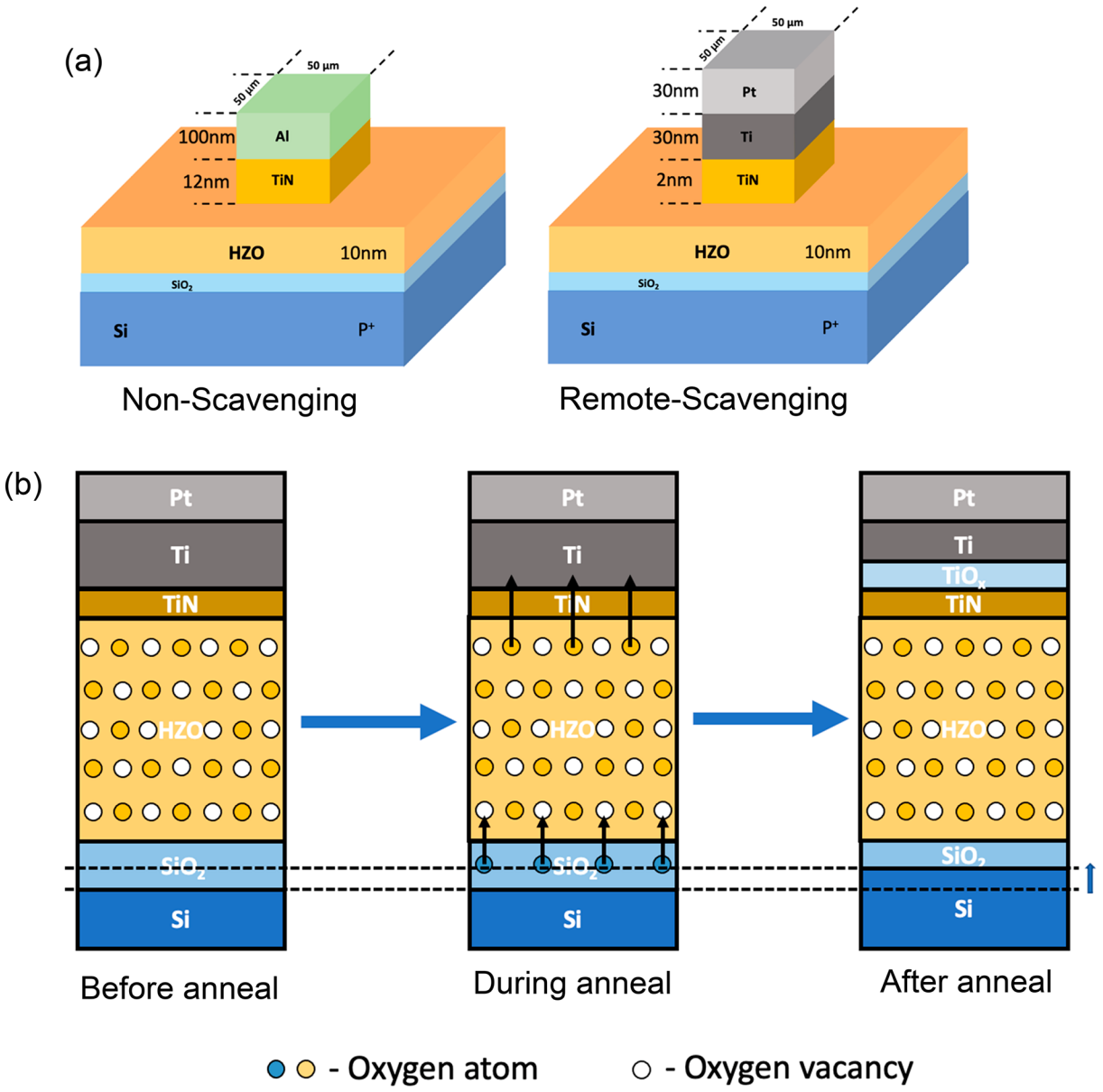

Figure 1. Device structure and oxygen scavenging model. (a) Device structures for nonscavenging and remote scavenging samples. (b) Oxygen scavenging mechanism enabled by oxygen vacancies in the HZO film which become mobile during high temperature anneal and allow net migration of oxygen atoms from the SiO_2 IL to the Ti layer to form TiO_x. Vacancies become mobile during high temperature anneal. Note that the thicknesses of the various layers are not to scale.

efficiency, FEFETs are an emerging nonvolatile memory technology for embedded and stand-alone applications.[9,10]

FEFET technology faces a critical challenge with respect to its write voltage, i.e., the voltage required to switch ferroelectric polarization in the FEFET structure. State-of-the art, Si-based FEFETs require at least 3−6 V for deterministic switching.[9−13] Conversely, for compatibility with logic circuits in embedded applications, the write voltage needs to be decreased below 1.5 V.[5] This challenge arises in part because during the deposition of the ferroelectric layer on Si in the standard transistor fabrication processes, an interfacial SiO_2 layer forms. Due to the low dielectric constant (~4) of the SiO_2 interfacial layer (IL), there is a large drop in the gate voltage across the IL which increases the write voltage to a value much higher than the coercive voltage of the equivalent, stand-alone ferroelectric layer. Reducing the thickness of the IL or eliminating it altogether has been suggested as one of the key strategies to reduce the write voltage in FEFETs.[5,14,15]

Techniques to reduce the IL thickness, often referred to as oxygen scavenging, were investigated in the context of the high-*k*-metal-gate technology development for standard complementary metal−oxide−semiconductor (CMOS) transistors, to reduce the effective oxide thickness (EOT) and improve the on-current.[16−18] Previous studies on amorphous dielectric (DE) HfO_2 gate oxides have successfully demonstrated significant EOT reduction by employing remote scavenging (sometimes called gettering) metal electrodes for SiO_2 IL scavenging.[16,19−21] Scavenging of interfacial SiO_2 occurs by depositing a reactive top metal gate such as Ti as shown in Figure 1a. Oxygen undergoes net migration from SiO_2 IL to Ti layer to form TiO_2, and thereby, the IL thickness is reduced. A thin TiN layer was added at the interface as a

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ACS Appl. Mater. Interfaces 2022, 14, 43897−43906

diffusion barrier to prevent the reactive metal from being incorporated into the HZO.[16] According to earlier studies on scavenging electrodes,[16] TiN is neutral and does not result in IL scavenging or regrowth (additional evidence shown in the Supporting Information, Figure S1). However, when the thickness of TiN is optimized and is used in conjunction with a reactive metal such as Ti, it can allow oxygen scavenging (evident in Figure 2) without permitting Ti diffusion into high-

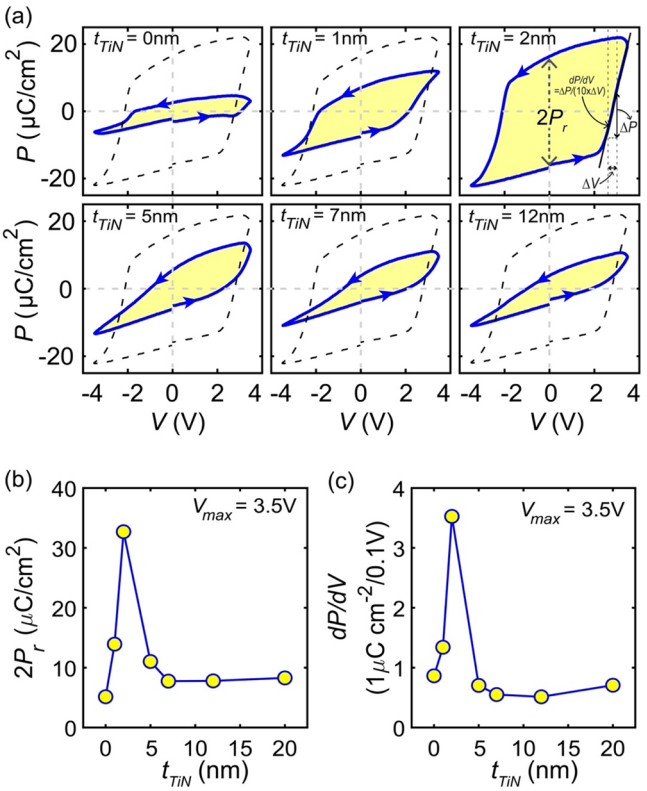

Figure 2. Optimization of the remote scavenging effects with a varying TiN thickness (t_{TiN}). (a) $P-V$ hysteresis loops of the remotely scavenged MOSCAPs for varying TiN thicknesses. The hysteresis curve for the MOSCAP with 2 nm TiN is shown in dotted lines for comparison with other MOSCAPs with different TiN thicknesses. Evolution of (b) switched polarization ($2P_r$) and (c) dP/dV with respect to TiN thicknesses. These parameters were extracted from the $P-V$ loops of the samples as shown in part (a) for the MOSCAP with 2 nm TiN (top right panel).

k causing leakage and work function shift. The Gibbs free energy change at 1000 K (ΔG^0 1000/O) for the following reaction is near zero for TiN, and therefore, a reactive metal (M) is needed.

$$\mathrm{Si} + \frac{2}{y}\mathrm{M}_x\mathrm{O}_y \rightarrow \frac{2x}{y}\mathrm{M} + \mathrm{SiO}_2 \quad (1)$$

The following chemical reaction for the reduction of SiO_2 can occur spontaneously due to the higher formation enthalpy of TiO_2 ($\Delta H^{\circ}_{f,solid}$ = −945 kJ/mol) than SiO_2 ($\Delta H^{\circ}_{f,solid}$= −911 kJ/mol):

$$\mathrm{Ti} + \mathrm{SiO}_2 \rightarrow \mathrm{Si} + \mathrm{TiO}_2 \quad (2)$$

It is noted that a suboxide reaction may also occur such as Ti + SiO → Si + TiO, but the thermodynamics is more difficult to quantify. Although reaction 1 is exothermic, kinetics plays a crucial role because the O atoms should migrate from the IL to the scavenging electrode through the HZO and TiN layers. Note that this is net transport; i.e., different oxygen atoms move from the IL to the HZO than from the HZO to the Ti layer. Oxygen vacancies in the HZO layer should be important in facilitating oxygen transport as shown in Figure 1b.[16,19,20] The scavenging electrode has also been reported to increase the dielectric constant of the HfO_2.[21]

In this study, a remote scavenging electrode of Ti was employed with a thin 2 nm TiN capping layer to study the effects of IL scavenging in ferroelectric metal−oxide−semiconductor (FE-MOS) capacitor structures. The prototype ferroelectric devices using HZO on highly doped Si has been reported previously.[14,32] When compared with MOS devices with conventional thick TiN electrodes, the remote scavenging electrode devices show a significant reduction in IL thickness resulting in a lower switching voltage and a 2× increase in remnant polarization (P_r) compared to a conventional device. These results are consistent with DFT modeling showing that the interlayer screens the electric field from the ferroelectric thereby decreases the field inside the semiconductor electrode and increases the voltage required for switching.

EXPERIMENTAL PROCEDURE

Ferroelectric HZO based MOS capacitors were fabricated using a p+Si(100) substrate with 10^{20} cm^{-3} doping concentration. Samples were dipped in HF to remove native oxide followed by 1.5 nm SiO_2 growth in SC-1 solution (5:1:1 NH_4OH:H_2O_2:H_2O). Then 10 nm of $Hf_{0.5}Zr_{0.5}O_2$ was deposited by thermal atomic layer deposition (ALD) at 250 °C in a Veeco Fiji G2 ALD system using tetrakis-(dimethylamido)hafnium, tetrakis(dimethylamido)zirconium, and H_2O precursors (Hf, Zr pulse time = 125 ms, H_2O pulse time = 60 ms, purge time = 10 s). Remote scavenging electrodes were deposited using 2−12 nm of TiN, 30 nm of Ti and 30 nm of Pt. Control samples with conventional electrodes were also made with 12 nm TiN and 100 nm Al. TiN was deposited in a different reactor by plasma enhanced ALD (PEALD) at 250 °C using tetrakis (dimethylamido)-titanium and N_2 plasma. Our ALD tool is a Veeco Fiji G2 ALD system with repeatable thickness control of ≤0.5 nm. Nucleation period for ALD TiN is small. Hence the films deposited using it (HZO, TiN layer) should be uniform and continuous. A post-TiN metallization annealing was performed at 450 °C for 30 s in a nitrogen atmosphere to crystallize the HZO. Ti, Pt and Al metals were deposited using electron beam evaporation through a shadow mask to define gates. Exposed TiN was etched using 5:1 H_2O:H_2O_2 at 50 °C to electrically isolate the gates. The samples were finally annealed in forming gas at 400 °C for 30 min. The two device structures are shown in Figure 1a.

The $P-V$ and $C-V$ characteristics were measured using an aixACCT TF-3000 ferroelectric parameter analyzer and an impedance analyzer (E4990A), respectively. Triangular pulses were applied to characterize the MOS capacitor's polarization charge vs voltage ($P-V$) loops at 1 kHz and 1.6 kHz to employ dynamic leakage current compensation (DLCC). DLCC is a feature in the aixACCT tool which is used mainly on leaky thin-film ferroelectric capacitors to separate switching current and dielectric displacement current from the leakage current. The key idea is to determine the ac current response of the sample for two adjacent frequencies and eliminate the leakage current based on that.[22] Details on the DLCC method are given in the Supporting Information (see Figure S2 and related text). $C-V$ was measured at 100 kHz frequency. Scanning transmission electron microscopy (STEM) and energy dispersion X-ray spectroscopic was performed on a FEI Talos F200X microscope equipped with Super X quadrant EDX detector, operated at 200 kV. The grazing incidence X-ray diffraction (GIXRD) measurements were carried out at the SLAC National Accelerator Laboratory using the Beamline 2−1 station with a Pilatus 100 K detector. An X-ray energy

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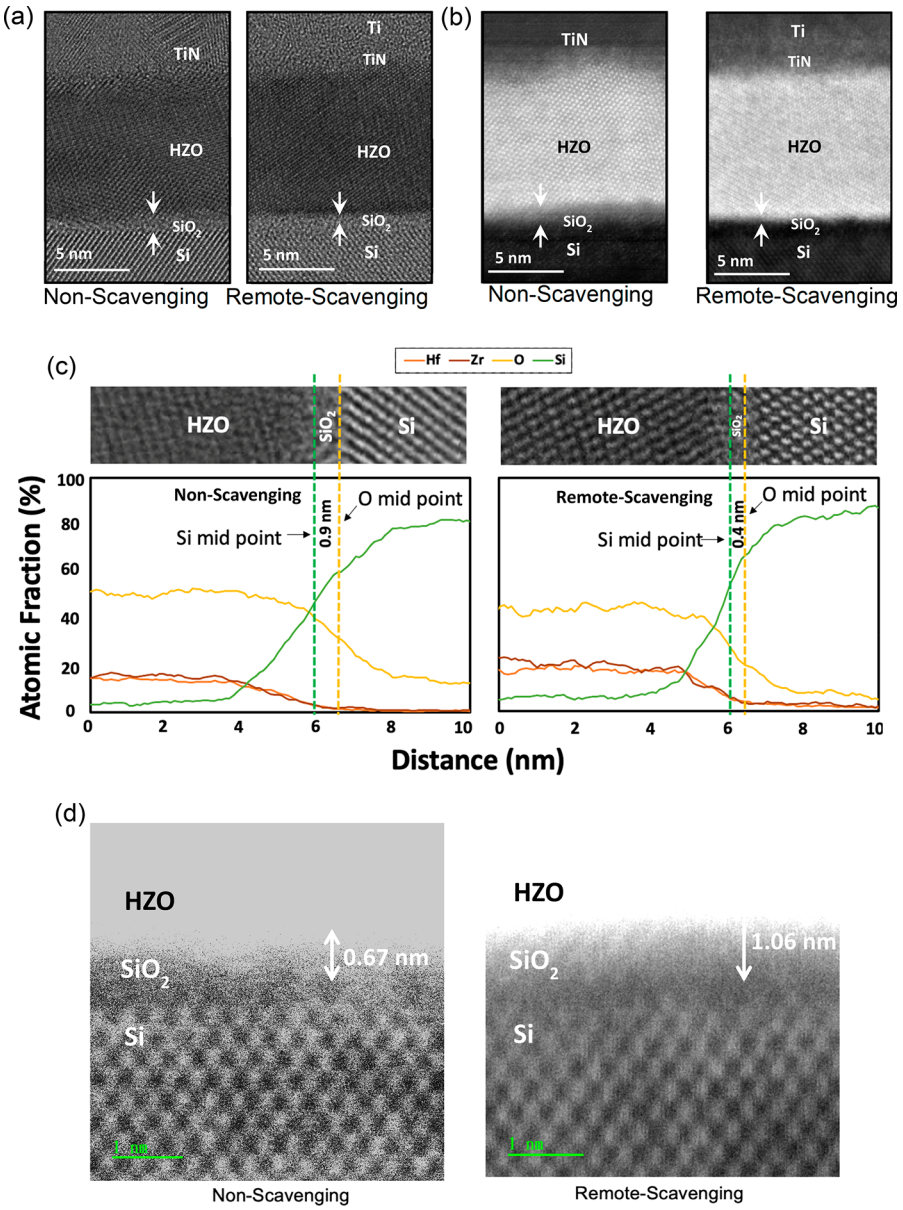

Figure 3. Microstructural characterizations based on TEM and EDS: (a) Bright-field TEM scans for nonscavenging (left) and scavenging (right). (b) *Z*-contrast images for nonscavenging (left) and scavenging (right). (c) EDS line trace for nonscavenging (top) and scavenging (bottom) samples at the HZO/SI interface. Remote-scavenging sample shows a 2× reduction in O−Si overlap region suggesting an IL reduction. The line traces are average of composition of 10 of the interface, and two separate regions on each samples were analyzed to confirm the elemental distribution. (d) Atomic resolution scanning TEM (STEM) image of remotely scavenged (left) and nonscavenged samples (right). The different brightness of two figures is caused by carbon contamination and charge accumulation.

of 17 keV (wavelength of 0.729 Å) was used, with X-rays incident to the HZO films at an angle of 0.15 deg.

COMPUTATIONAL DETAILS

Density functional theory (DFT) was employed to explain the effects of DE IL thickness scaling in the MFIS stacks. For simplicity, Ni was used as a metal electrode in the place of TiN, and cubic HZO ($Fm\bar{3}m$) served as a model dielectric in the place of SiO_2. The simpler models used in this study are advantageous to isolate the electrostatic effects, which are dominant in this case, from bond strains, and the validity of the simple models was described previously.[23]

The plane-wave basis set was used to represent electron wave functions with a kinetic energy cutoff of 400 eV, and the projector augmented wave method[24] was used for the core part of the pseudopotential. The exchange-correlation functional of Perdew−Burke−Ernzerhof[25] was employed for the Kohn−Sham Hamiltonian. The Monkhorst−Pack[26] scheme was employed for Brillouin zone integration on a 6 × 6 × 1 grid. The self-consistent field and ionic relaxation were performed until the stopping criteria of 10^{-4} meV and 1 meV/Å, respectively. All the DFT calculations were performed by using the Vienna *Ab Initio* Software Package.[27,28]

RESULTS AND DISCUSSION

Scavenging electrode structures with 0−12 nm TiN thicknesses were characterized to determine the optimal TiN thickness. Figure 2a shows the *P*−*V* response for the various scavenging electrode devices. The device with 0 nm TiN shows

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low P_r. This may be due to aggressive direct oxygen scavenging by Ti in absence of a TiN layer. This may lead to oxygen vacancies in HZO which can pin the ferroelectric grain or induce a phase change thereby reducing the P_r. By inspection, the 2 nm films in Figure 2a show nearly ideal ferroelectric behavior with a steep turn on and turn off and a higher $2P_r$. All the $P-V$ loops shown in Figure 2a were determined at ±4 V and the data is consistent with the 2 nm film sample reaching its major loop at this voltage while the other samples' $P-V$ loops are not fully saturated. This indicates that the write voltage is much smaller in the sample with 2 nm TiN.

To quantitatively compare the electrical characteristic as a function of TiN thickness, the steepness of switching is quantified from the slopes of P vs V; this is denoted as dP/dV. Figure 2b summarizes the $2P_r$ and dP/dV values for the different TiN thicknesses. The sample with 2 nm TiN shows the highest P_r, and it decreases for thicker TiN. This suggests that thinner TiN enables more oxygen diffusion to Ti layer causing greater IL reduction. 2 nm TiN sample was chosen as the prime candidate for further characterization. The GIXRD pattern shown in Figure S3 or the leakage current in Figure S4 cannot explain the sharp $2P_r$ maximum in the 2 nm TiN sample shown in Figure 2. To reveal the underlying reasoning behind it, further investigation in required, including studying the effect of charge trapping-detrapping at the IL/HZO interface.

The samples with scavenging and nonscavenging electrode were characterized by transmission electron microscopy (TEM) as shown in parts a and b of Figure 3. The nonscavenging sample shows polycrystalline HZO with only occasional zone alignment with the underlying substrate. In addition, the nonscavenging sample has a clearly visible amorphous SiO_2 layer of about 1 nm thickness; the thickness is quantified below using elemental analysis. TEM images were recorded in three different locations (see Figure S5).

The Energy Dispersion Spectroscopy (EDS) elemental analysis in Figure 3c provides a clear image of the effect of IL scavenging. The signal is averaged over a 10 nm distance to reduce noise; two separate regions on each sample were analyzed to confirm the elemental distribution. The midpoints of EDS line traces for Hf, Zr, Ti, N, Si, and O were identified (see Figure S6). The scavenging electrode sample shows a 0.4 nm separation in the Si and O regions at the HZO/Si interface compared to a 0.9 nm separation for the nonscavenging electrode, suggesting at least a 50% reduction in the IL. The reduction of the IL can be attributed to the net migration of O atoms from the SiO_2 IL to the Ti scavenging layer to form TiO_x as dictated by the negative Gibbs free energy change in eq 1. The data is consistent with the thick TiN layer in the nonscavenging device preventing O atoms from reaching the Al metal layer and therefore does not result in the IL thinning observed for the scavenging electrode device.

For both devices, The Ti, Hf, and Zr midpoints coincide at the TiN/HZO interface, confirming absence of Ti diffusion into HZO (see Figure S6). The nonscavenging device does show some N diffusion in HZO. Spectrum images were obtained to further investigate the Ti/O ratio in the scavenging sample, which is shown in Figure S7 of the Supporting Information. The dependence of the oxygen content on the lamella size indicates that a major part of this oxygen comes from the atmosphere during lamella preparation. This atmospheric oxygen makes it difficult to distinguish the diffusion of the comparatively smaller amount of oxygen from the IL to Ti metal due to scavenging. The details of the investigation are described in the Supporting Information.

The atomic resolution STEM images shown in Figure 3d depicts that SiO_2 layer thickness is 0.67 and 1.07 nm for the scavenged and nonscavenged sample, respectively. The corresponding STEM line intensity profile is shown in the Supporting Information (Figure S8). Due to the problematic nature of measuring the dielectric film with thickness around 0.5 nm in nonaberration correction TEM,[34] it is possible that the true thickness of our interlayer oxide may be even lower than 0.67 nm.

Devices were electrically characterized after 10^3 wake-up cycles. Over 20 devices were measured on each sample and Figure 4a shows representative $C-V$ from two separate

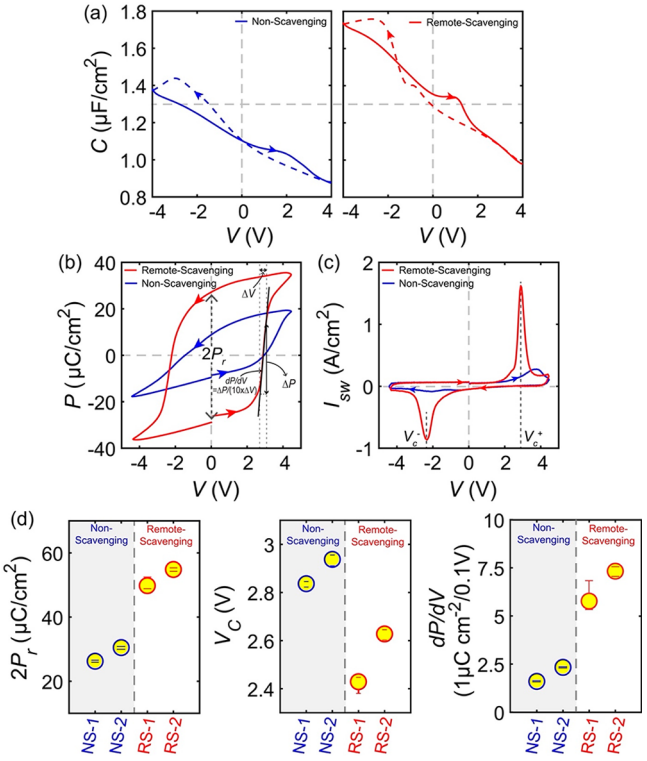

Figure 4. Electrical Characterizations of remote scavenging and nonscavenging devices: (a) $C-V$ (b) $P-V$, and (c) $I_{sw}-V$ for nonscavenging and scavenging samples. Switched polarization, $2P_r$ and change in polarization w.r.t. voltage, dP/dV are indicated in part b, while the coercive voltages, V_c^+ and V_c^- ($V_c = (V_c^+ + V_c^-)/2$) are indicated in part c for the remotely scavenged samples Two samples were fabricated without applying the scavenging technique on them (NS-1, NS-2) and two were fabricated using emote scavenging (RS-1, RS-2). (d) Evolution of $2P_r$, V_c, and dP/dV for remote-scavenging (RS) and nonscavenging (NS) samples. The error bars in part d represent the difference in the parameters obtained from different devices on the same sample. The maximum voltage (V_{max}) applied to both samples is 4.5 V.

samples of each type. The 25% increase in accumulation capacitance with the scavenging electrode is consistent with the effect of IL reduction. The $P-V$ loops were measured by applying 0.6−1 ms triangular pulses whereas a DC sweep was used in the impedance analyzer to measure the $C-V$. V_c depends on the rate of change of voltage, dV/dt in an MOS structure.[33] As dV/dt increases, i.e., the sweep time decreases, V_c increases with it. Hence the slower sweep in $C-V$ could

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Table 1. Dielectric Constant of the FE Layer

device	C at 0 V (μF/cm^2)	CET = $\epsilon_o\epsilon_{IL}/C$ (nm)	t_{IL} (nm)	EOT = CET − t_{IL} − 0.3 nm (nm)	ϵ_{FE} = (t_{FE}/EOT)ϵ_{IL}
nonscavenging	1.1	3.14	1.1	2.07	22.4
scavenging	1.32	2.62	0.7	1.62	24.1

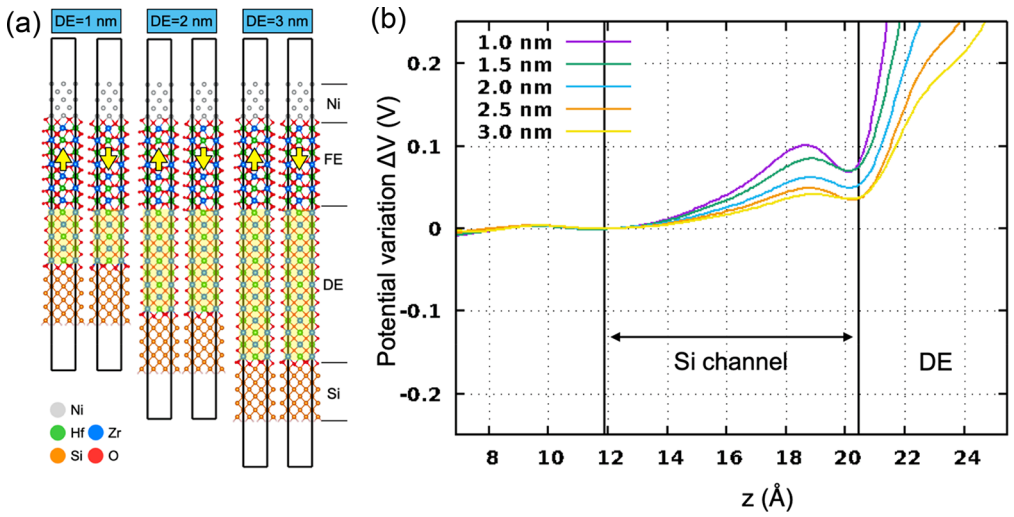

Figure 5. DFT models of MFIS stacks with a varying DE thickness. (a) Atomic models of metal−ferroelectric-insulator−semiconductor stacks with a varying dielectric thickness. (b) Potential variation (ΔV) in the Si channel region due to polarization switching as a function of DE thickness. The larger ΔV in the Si channel with thinner DE layer indicates the larger memory window in the FEFET devices.

have led to lower V_c values in $C-V$ curves compared to the ones from $P-V$ curves as shown in Figure 4a,b.

Similar phenomenon for an MOS structure (metal−oxide−semiconductor) can also be observed in another report.[30] From the capacitance vs voltage ($C-V$) curves in Figure 4a, we can evaluate the capacitive equivalent thickness (CET) using the equation CET = $\epsilon_o\epsilon_{IL}/C$, where ϵ_{IL} = 3.9 is the dielectric constant of SiO_2 and C is the capacitance of the MOSCAP (as shown in Figure 4a). As evident from Figure 3c,d and Figure S9, the IL thickness (t_{IL}) of the remote-scavenging is lower than the nonscavenging sample. Next the equivalent oxide thickness (EOT) from CET and t_{IL} using EOT = CET − t_{IL} − 0.3 nm (additional 0.3 nm is deducted for quantum correction). Finally, the dielectric constant of the HZO layer can be calculated from ϵ_{FE} = (t_{FE}/EOT)ϵ_{IL} (thickness of the HZO layer, t_{FE} = 10 nm). The calculation is shown in Table 1, using t_{IL} determined from STEM (Figure 3d and Figure S9):

$P-V$ measurements in Figure 4b show a 2× increase (~20 to ~50 μC/cm^2) in remanent polarization ($2P_r$) for the devices with a scavenging electrode compared to the conventional devices. The lower switching voltage V_c (extracted from the peaks of the switching current, I_{sw}, vs voltage curves) of the scavenging sample is also consistent with EOT reduction. The minor hysteretic $P-V$ loops (Figure S10) and the positive-up−negative-down (PUND) measurements (Figure S11) provide additional evidence to the decrease in the write voltage with scavenging. Both minor $P-V$ loops (Figure S10) and the PUND measurement (Figure S11) reveal that the non-scavenged sample goes to a major loop (i.e., fully polarizes) at a write voltage of around 4.5−5 V while the remotely scavenged sample fully polarizes earlier, at around 3.5 V. The greater $2P_r$ for the scavenging samples is unlikely due to conversion of tetragonal to orthorhombic phase since there is no hint of antiferroelectric behavior in the $P-V$ of the sample with a standard gate. Additionally, the GIXRD patterns shown in Figure S3 indicate that the HZO film in both the samples are orthorhombic. The increase in remanent polarization with the scavenging electrode may be due to filling of oxygen vacancies in the HZO film due the migration of oxygen atoms from IL to Ti scavenging layer during scavenging process. Filling up of oxygen vacancies in orthorhombic crystal would cause depinning of FE grains and demonstrate an enhancement in polarization. The nature of the $2P_r$ in the nonscavenged and scavenged sample could originate from the internal depolarization field coupled with charge trapping/detrapping at the defect states at the FE-HZO/p+Si interface.[31] Note that it is difficult to compare the two cases quantitatively due to the different thicknesses of the ILs. Further investigation is required to understand the depolarization field's effect on the $2P_r$ values of these samples.

It is noted that the inclusion of the Pt layer in the scavenging sample has no effect on the electrical characteristics which is evident from Figure S12 in the Supporting Information. The reason for using different top electrode stacks for scavenging and nonscavenging is due to a trade-off. The common metals that are good oxygen diffusion barriers have a high binding energy to oxygen, so they might also scavenge the oxygens from the interlayer. For the sample with the Ti scavenging layer, an inert metal (Pt) was used for the gate electrode to ensure all the scavenging effects occurred solely by the Ti layer. For the nonscavenging sample, an Al gate electrode was employed to avoid any oxygen penetration into the film.

Even though the oxygen migration possibly occurs by filling up the oxygen vacancies in the HZO film, the remotely scavenged sample demonstrates a higher amount of gate leakage than the nonscavenged one (Figure S4, Supporting Information). This is because the thinning of IL should have a greater impact on gate leakage because gate leakage is sensitive to the amorphous low-k SiO_2 interlayer thickness and

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scavenging electrodes have been reported to increase gate leakage when compared to devices with thicker ILs.[31]

To test the repeatability of the process, two sets of scavenging and nonscavenging electrode samples were fabricated and 5 devices on each sample were measured. The results are summarized in Figure 4d. The device-to-device variation on each sample shown by the error bars is not significant. The two sets of data from different samples show similar P_r, V_c, and dP/dV. Figure 4c clearly shows the 2× increase in $2P_r$ and the decrease in V_c in the remotely scavenged sample compared to the nonscavenged sample even for two different sets of samples.

Another parameter, dP/dV, is also plotted in the last panel of Figure 4d for all the samples, which represents the steepness of switching as indicated in the $P-V$ loop for the remotely scavenged sample shown in Figure 4b. It is evident from the last panel of Figure 4d that the steepness of switching (dP/dV) is higher in the remotely scavenged sample compared to the nonscavenged sample. The polarization increases by 6.5−7.5 $\mu C/cm^2$ with a 0.1 V increase in the remotely scavenged samples whereas it increases by only ∼2.5 $\mu C/cm^2$ with the same amount of voltage increase (0.1 V) in the nonscavenged sample.

A systematic study of first-principles DFT calculations of the effect of IL thinning is shown in Figure 5a. Metal-ferroelectric-insulator-semiconductor (MFIS) stack models with a varying DE IL thickness are developed here to investigate the scavenging effects. For simplicity, Ni was used as a metal electrode (in the place of TiN), while cubic HZO was used to represent the DE IL (in the place of SiO_x). Charge compensation by the metal electrode and interfacial bonding between FE and DE IL layers are less ideal in the TiN/HZO/SiO_2/Si structure, but electrostatic effects play a crucial role, and the simple models employed here are suitable for describing the scaling behaviors in the MFIS stacks as described previously.[23] The DFT model here confirms the crucial role of the IL thickness in the MFIS stack structures without an empirical parameter."

Unlike the finite DE IL, ultrathin DE IL at the FE−DE interface would enhance the stability of the FE orthorhombic phase, enhancing the FE characteristics of the device as shown in Figure 4. The electrostatic interactions between FE and DE layers induce internal field in the FE layer and the depolarization field in the adjacent DE layer. The strength of the induced depolarization field increases with a decreasing DE thickness, but both polarization and depolarization fields are significantly reduced when the IL is completely removed.[23] It is noted that aggressive remote-scavenging might allow non-stoichiometric SiO_x ($x < 2$) suboxide formation or local regions of direct contact between the HZO and Si substrate, which diminishes internal field induction and promotes the FE phase. In addition to the improved FE properties such as enhanced $2P_r$ and reduced V_c, the potential modulation in the silicon channel region, which is analogous to the memory window, due to the polarization switching ($\Delta V = V_{up}^{Si} - V_{down}^{Si}$) is increased monotonously due to the decreasing IL thickness as shown in Figure 5b. This is attributed to the reduced electrostatic screening by the DE layer as its thickness gets thinner and is desirable for lower operation voltage. Conversely, the size of the depolarization field in the DE layer increases with thinning the IL thickness, or scavenging process, as shown previously.[23] This would generate excessive defects at the FE/DE interface and result in the material failure earlier, consistent with the observation in Figure S13.

It can be noted that how to balance the trade-off between write voltage and endurance in FEFETs is application dependent. For example, for Artificial Intelligence (AI) inference engines (the most dominant application in hard AI), logic compatible voltages and density are of utmost importance, and the write operations are sporadic (and hence the write endurance is of less importance). In such applications, increase in the write voltage above logic compatible levels requires level-shifters, which reduce the density of the memory array. How scavenging-based technique to reduce write voltage fits to different application domains will require application-level benchmarking considering all aspects, including write voltage, endurance, and speed, read speed and endurance, retention, and so on. It is worth noting that ferroelectric field-effect transistors are primarily a FLASH replacement for embedded nonvolatile memory applications, due to their superior energy profile and scalability (FEFET, 7 nm node and beyond, vs FLASH, 28/22 nm). FLASH technology has a limited write endurance of around 1000 cycles and hence limited FEFET endurance does not represent a showstopper for technology adoption.

It can be further noted that endurance in FEFETs is affected by multiple effects, and two-terminal measurements of FE MOS capacitors, as presented herein, does not represent the complete picture. Most importantly, write endurance is significantly affected by the carrier type in the semiconductor channel. The presence of holes in the channel degrades the endurance most significantly as we have shown recently.[29] On the other hand, back end of the line (BEOL) FEFETs with non-Si channel such as with In_2O_3 channel, operating in depletion[14] or fully depleted FEFETs,[30] have much higher endurance. In other words, complete assessment of endurance properties needs to be performed in FEFET structures with scavenged oxides (not in FE MOS capacitors).

CONCLUSION

Remote scavenging electrode can be employed to scavenge oxygen from SiO_2 IL for a FE MOS device. A 2× increase in P_r and sharper switching compared to conventional device was observed. The oxygen scavenging reduces EOT by thinning IL. The internal field becomes significant when the DE layer is reduced to a few nanometers (<3 nm). This partly explains the enhanced ferroelectric properties in MOS structure with remote scavenging electrodes. In addition to the improved FE properties such as enhanced $2P_r$ and reduced $\Delta V = V_{up}^{Si} - V_{down}^{Si}$ the potential modulation in the silicon channel region, which is analogous to the memory window, due to the polarization switching increased monotonously due to the decreasing IL thickness. This is attributed to the reduced electrostatic screening by the DE layer as its thickness gets thinner and is desirable for lower operation voltage. Conversely, the size of the depolarization field in the DE layer increases with thinning the IL thickness, or gettering process, as shown previously.[23] Given the need for reducing the write voltage in ferroelectric field-effect transistors, state-of-the-art interfacial passivation techniques[31] can be employed to mitigate the adverse effects of remote scavenging to thin down the interfacial layer in these devices.

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■ ASSOCIATED CONTENT

Supporting Information

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Additional evidence of TiN being neutral and not affecting scavenging process (Figure S1), details on the DLCC method (Figure S2), GIXRD patterns (Figure S3) and leakage current (Figure S4) of the samples, TEM images recorded in three different locations (Figure S5) and EDS line traces (Figure S6) of the samples, HAADF TEM cross sectional images of the samples, full EDS spectrum and elemental compositions of lamellae (Figure S7), atomic resolution STEM images and STEM line intensity profiles (Figure S8), STEM and EDS line profile measurements (Figure S9) and minor *P*−*V* loops (Figure S10) of the samples, PUND measurement (Figure S11), evidence of inclusion of the Pt layer that has no effect on the scavenging sample (Figure S12), endurance measurement (Figure S13) and EDS elemental composition analysis (Figure S14) of the samples, and electric field calculation in HZO films using a simple electrostatic model (pp S15−S16) (PDF)

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Notes

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REFERENCES

(1) Böscke, T. S.; Teichert, St.; Bräuhaus, D.; Müller, J.; Schröder, U.; Böttger, U.; Mikolajick, T. Phase Transitions in Ferroelectric Silicon Doped Hafnium Oxide. *Appl. Phys. Lett.* **2011**, *99* (11), 112904.

(2) Boscke, T. S.; Muller, J.; Brauhaus, D.; Schroder, U.; Bottger, U. Ferroelectricity in Hafnium Oxide: CMOS Compatible Ferroelectric Field Effect Transistors. In *2011 International Electron Devices Meeting*; IEEE: Washington, DC, USA, 2011; p 24.5.1−24.5.4; DOI: 10.1109/IEDM.2011.6131606.

(3) Mikolajick, T.; Schroeder, U.; Slesazeck, S. The Past, the Present, and the Future of Ferroelectric Memories. *IEEE Trans. Electron Devices* **2020**, *67* (4), 1434−1443.

(4) Wong, J. C.; Salahuddin, S. Negative Capacitance Transistors. *Proc. IEEE* **2019**, *107* (1), 49−62.

(5) Khan, A. I.; Keshavarzi, A.; Datta, S. The Future of Ferroelectric Field-Effect Transistor Technology. *Nat. Electron* **2020**, *3* (10), 588−597.

(6) Yu, S.; Hur, J.; Luo, Y.-C.; Shim, W.; Choe, G.; Wang, P. Ferroelectric HfO_2 -Based Synaptic Devices: Recent Trends and Prospects. *Semicond. Sci. Technol.* **2021**, *36* (10), 104001.

(7) Ma, T. P.; Jin-Ping Han. Why Is Nonvolatile Ferroelectric Memory Field-Effect Transistor Still Elusive? *IEEE Electron Device Lett.* **2002**, *23* (7), 386−388.

(8) Muller, J.; Polakowski, P.; Riedel, S.; Mueller, S.; Yurchuk, E.; Mikolajick, T. Ferroelectric Hafnium Oxide A Game Changer to FRAM? In *2014 14th Annual Non-Volatile Memory Technology Symposium (NVMTS)*; IEEE: Jeju Island, 2014; pp 1−7; DOI: 10.1109/NVMTS.2014.7060838.

(9) Trentzsch, M.; Flachowsky, S.; Richter, R.; Paul, J.; Reimer, B.; Utess, D.; Jansen, S.; Mulaosmanovic, H.; Muller, S.; Slesazeck, S.; Ocker, J.; Noack, M.; Muller, J.; Polakowski, P.; Schreiter, J.; Beyer, S.; Mikolajick, T.; Rice, B. A 28nm HKMG Super Low Power Embedded NVM Technology Based on Ferroelectric FETs. In *2016 IEEE International Electron Devices Meeting (IEDM)*; IEEE: San Francisco, CA, 2016; p 11.5.1−11.5.4; DOI: 10.1109/IEDM.2016.7838397.

(10) Dünkel, S.; Trentzsch, M.; Richter, R.; Moll, P.; Fuchs, C.; Gehring, O.; Majer, M.; Wittek, S.; Müller, B.; Melde, T.; Mulaosmanovic, H.; Slesazeck, S.; Müller, S.; Ocker, J.; Noack, M.; Müller, J.; Mikolajick, T.; Höntschel, J.; Rice, B.; Pellerin, J.; Beyer, S. A FeFET Based Ultra-Low-Power Ultra-Fast Embedded NVM Technology for 22nm FDSOI and Beyond. *2017 IEEE International Electron Devices Meeting (IEDM)* 2017; DOI: 10.1109/IEDM.2017.8268425

(11) Tan, A. J.; Yadav, A. K.; Chatterjee, K.; Kwon, D.; Kim, S.; Hu, C.; Salahuddin, S. A Nitrided Interfacial Oxide for Interface State Improvement in Hafnium Zirconium Oxide-Based Ferroelectric Transistor Technology. *IEEE Electron Device Lett.* **2018**, *39* (1), 95−98.

(12) Tasneem, N.; Islam, M. M.; Wang, Z.; Chen, H.; Hur, J.; Triyoso, D.; Consiglio, S.; Tapily, K.; Clark, R.; Leusink, G.; Yu, S.; Chern, W.; Khan, A. The Impacts of Ferroelectric and Interfacial Layer Thicknesses on Ferroelectric FET Design. *IEEE Electron Device Lett.* **2021**, *42* (8), 1156−1159.

(13) Saitoh, M.; Ichihara, R.; Yamaguchi, M.; Suzuki, K.; Takano, K.; Akari, K.; Takahashi, K.; Kamiya, Y.; Matsuo, K.; Kamimuta, Y.; Sakuma, K.; Ota, K.; Fujii, S. HfO2-Based FeFET and FTJ. for Ferroelectric-Memory Centric 3D LSI towards Low-Power and High-Density Storage and AI Applications. *2020 IEEE International Electron Devices Meeting (IEDM)*; 2020; DOI: 10.1109/IEDM13553.2020.9372106

(14) Dutta, S.; Ye, H.; Khandker, A. A.; Kirtania, S. G.; Khanna, A.; Ni, K.; Datta, S. Logic Compatible High-Performance Ferroelectric Transistor Memory. *IEEE Electron Device Lett.* **2022**, *43* (3), 382−385.

(15) Ni, K.; Sharma, P.; Zhang, J.; Jerry, M.; Smith, J. A.; Tapily, K.; Clark, R.; Mahapatra, S.; Datta, S. Critical Role of Interlayer in $Hf_{0.5}Zr_{0.5}O_2$ Ferroelectric FET Nonvolatile Memory Performance. *IEEE Trans. Electron Devices* **2018**, *65* (6), 2461−2469.

(16) Ando, T. Ultimate Scaling of High-κ Gate Dielectrics: Higher-κ or Interfacial Layer Scavenging? *Materials* **2012**, *5* (12), 478−500.

(17) Huang, J. 3A-1 Gate First High-k/Metal Gate Stacks with Zero SiOx Interface Achieving EOT = 0.59nm for 16nm Application. *2009 Symposium on VLSI Technology* **2009**, 34−35.

(18) Marchiori, C.; Frank, M. M.; Bruley, J.; Narayanan, V.; Fompeyrine, J. Epitaxial SrO Interfacial Layers for HfO2-Si Gate Stack Scaling. *Appl. Phys. Lett.* **2011**, *98* (5), 052908.

(19) Kavrik, M. S.; Thomson, E.; Chagarov, E.; Tang, K.; Ueda, S. T.; Hou, V.; Aoki, T.; Kim, M.; Fruhberger, B.; Taur, Y.; McIntyre, P. C.; Kummel, A. C. Ultralow Defect Density at Sub-0.5 Nm HfO_2 /SiGe Interfaces via Selective Oxygen Scavenging. *ACS Appl. Mater. Interfaces* **2018**, *10* (36), 30794−30802.

(20) Kim, H.; McIntyre, P. C.; On Chui, C.; Saraswat, K. C.; Stemmer, S. Engineering Chemically Abrupt High-k Metal Oxide/silicon Interfaces Using an Oxygen-Gettering Metal Overlayer. *J. Appl. Phys.* **2004**, *96* (6), 3467−3472.

(21) Kwak, I.; Kavrik, M.; Park, J. H.; Grissom, L.; Fruhberger, B.; Wong, K. T.; Kang, S.; Kummel, A. C. Low Interface Trap Density in Scaled Bilayer Gate Oxides on 2D Materials via Nanofog Low Temperature Atomic Layer Deposition. *Appl. Surf. Sci.* **2019**, *463*, 758−766.

(22) Meyer, R.; Waser, R.; Prume, K.; Schmitz, T.; Tiedke, S. Dynamic Leakage Current Compensation in Ferroelectric Thin-Film Capacitor Structures. *Appl. Phys. Lett.* **2005**, *86* (14), 142907.

(23) Chae, K.; Kummel, A. C.; Cho, K. Hafnium-Zirconium Oxide Interface Models with a Semiconductor and Metal for Ferroelectric Devices. *Nanoscale Adv.* **2021**, *3* (16), 4750−4755.

(24) Kresse, G.; Joubert, D. From Ultrasoft Pseudopotentials to the Projector Augmented-Wave Method. *Phys. Rev. B* **1999**, *59* (3), 1758−1775.

(25) Perdew, J. P.; Burke, K.; Ernzerhof, M. Generalized Gradient Approximation Made Simple. *Phys. Rev. Lett.* **1996**, *77* (18), 3865−3868.

(26) Monkhorst, H. J.; Pack, J. D. Special Points for Brillouin-Zone Integrations. *Phys. Rev. B* **1976**, *13* (12), 5188−5192.

(27) Kresse, G.; Furthmüller, J. Efficient Iterative Schemes for *Ab Initio* Total-Energy Calculations Using a Plane-Wave Basis Set. *Phys. Rev. B* **1996**, *54* (16), 11169−11186.

(28) Kresse, G.; Furthmüller, J. Efficiency of Ab-Initio Total Energy Calculations for Metals and Semiconductors Using a Plane-Wave Basis Set. *Comput. Mater. Sci.* **1996**, *6* (1), 15−50.

(29) Wang, Z. Improved Endurance with Electron-Only Switching in Ferroelectric Devices. *Proceeding in Device Research Conference (DRC)* 2022; in press.

(30) Tan, A. J.; Liao, Y.-H.; Wang, L.-C.; Shanker, N.; Bae, J.-H.; Hu, C.; Salahuddin, S. Ferroelectric HfO_2 Memory Transistors With High- κ Interfacial Layer and Write Endurance Exceeding 10^{10} Cycles. *IEEE Electron Device Lett.* **2021**, *42* (7), 994−997.

(31) Nguyen, M.-C.; Kim, S.; Lee, K.; Yim, J.-Y.; Choi, R.; Kwon, D. Wakeup-Free and Endurance-Robust Ferroelectric Field-Effect Transistor Memory Using High Pressure Annealing. *IEEE Electron Device Lett.* **2021**, *42* (9), 1295−1298.
(32) Zacharaki, C.; Tsipas, P.; Chaitoglou, S.; Evangelou, E. K.; Istrate, C. M.; Pintilie, L.; Dimoulas, A. Depletion Induced Depolarization Field in $Hf_{1-x}Zr_xO_2$ Metal-Ferroelectric-Semiconductor Capacitors on Germanium. *Appl. Phys. Lett.* **2020**, *116* (18), 182904.
(33) Cheema, S. S.; Shanker, N.; Wang, L.-C.; Hsu, C.-H.; Hsu, S.-L.; Liao, Y.-H.; San Jose, M.; Gomez, J.; Chakraborty, W.; Li, W.; Bae, J.-H.; Volkman, S. K.; Kwon, D.; Rho, Y.; Pinelli, G.; Rastogi, R.; Pipitone, D.; Stull, C.; Cook, M.; Tyrrell, B.; Stoica, V. A.; Zhang, Z.; Freeland, J. W.; Tassone, C. J.; Mehta, A.; Saheli, G.; Thompson, D.; Suh, D. I.; Koo, W.-T.; Nam, K.-J.; Jung, D. J.; Song, W.-B.; Lin, C.-H.; Nam, S.; Heo, J.; Parihar, N.; Grigoropoulos, C. P.; Shafer, P.; Fay, P.; Ramesh, R.; Mahapatra, S.; Ciston, J.; Datta, S.; Mohamed, M.; Hu, C.; Salahuddin, S. Ultrathin ferroic HfO2−ZrO2 superlattice gate stack for advanced transistors. *Nature* **2022**, *604*, 65−71.
(34) Diebold, A.C.; Foran, B.; Kisielowski, C.; Muller, D.A.; Pennycook, S.J.; Principe, E.; Stemmer, S. Thin dielectric film thickness determination by advanced transmission electron microscopy. *Microscopy and Microanalysis* **2003**, *9*, 493−508.

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